#11/Appeal Brief 9-4-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Daniel WATKINS	§	Group Art Unit:	2857
Serial No.: 09/363,311	§	Examiner:	Mary C. BARAN
Filed: July 28, 1999	§	Atty. Dkt. No:	5201-16300
For: A Functional-Pattern Management System For Device Verification	§		

9/5 MSW

BOARD OF PATENT APPEALS AND INTERFERENCES
APPEAL BRIEF UNDER 37 C.F.R. 1.192

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Date: August 18, 2003

Dear Sir:

This paper is submitted as an appeal from a final rejection of claims 1-20 pursuant to a Notice of Appeal filed July 18, 2003.

Real Party In Interest

The real party in interest is the assignee: LSI Logic Corporation.

Related Appeals And Interferences

No other appeals or interferences are known to the applicants, the applicants' legal representative, or the assignee, that will directly affect or be directly affected by or have a bearing on the Board's decision in an appeal on this case.

Status Of Claims

Originally filed claims: 1-20.

Presently pending claims: 1-20.

Rejected claims: 1-20.

Status of Amendments

No amendments are pending in this case.

Invention Summary

The claims are directed to (among other things) a system and method for verifying the functionality of a device design. In previous approaches, the construction and handling of test patterns has proven to be difficult and unwieldy. The invention of claim 1 addresses this problem through the use of a pattern profile which can be generated, analyzed, and eventually converted into a test pattern by various system modules. Using the pattern profile allows for the efficient production of test patterns that are better understood by the user and that enable better coverage due to the use of a human-intelligible profile.

Claim 1 is reproduced below:

1. (Once amended) A system for device verification, wherein the system comprises

a profile generation module configured to provide a pattern profile that represents a sequence of input signal vectors with an associated sequence of output signal vectors (hereafter a "test pattern"), wherein the pattern profile includes a human-intelligible description of aspects of the test pattern, wherein the aspects are specified by a profile mode;

a coverage measurement module configured to process the pattern profile to produce analysis results indicative of coverage provided by the test pattern, wherein the profile generation module is further configured to process the analysis results to provide an improved pattern profile; and

a pattern generation module configured to receive the improved pattern profile and to convert the improved pattern profile into a test pattern for verifying device performance.

To aid in understanding of this claim, the various claim limitations are associated with portions of Fig. 3 in the diagram on the following page.

1. (Once amended) A system for device verification, wherein the system comprises

a profile generation module configured to provide a pattern profile that represents a sequence of input signal vectors with an associated sequence of output signal vectors (hereafter a "test pattern"), wherein the pattern profile includes a human-intelligible description of aspects of the test pattern, wherein the aspects are specified by a profile mode;

a coverage measurement module configured to process the pattern profile to produce analysis results indicative of coverage provided by the test pattern, wherein the profile generation module is further configured to process the analysis results to provide an improved pattern profile; and

a pattern generation module configured to receive the improved pattern profile and to convert the improved pattern profile into a test pattern for verifying device performance.

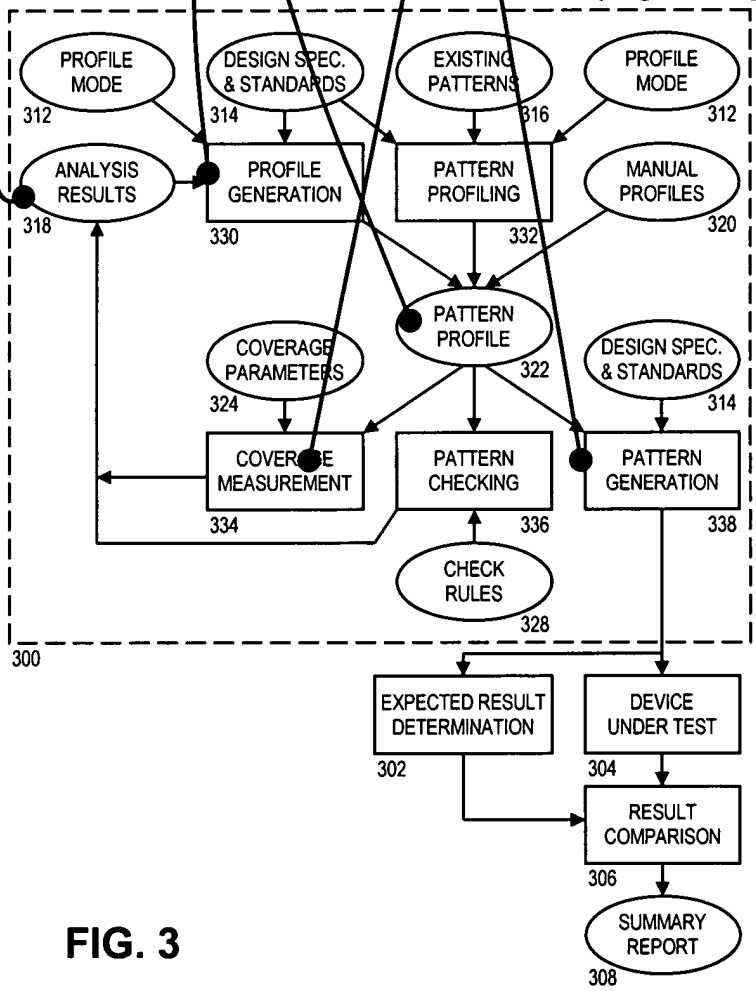


FIG. 3

Prior Proceedings

In the final office action mailed April 18, 2003, claims 1-6, 8-9, 11-14, and 16-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,949,691 ("Kurosaka") in view of U.S. Patent No. 6,141,630 ("McNamara"). Claims 7, 10, and 15 were rejected under 35 U.S.C § 103(a) as being unpatentable over Kurosaka in view of McNamara and U.S. Patent No. 5,684,808 ("Valind").

U.S. Patent No. 5,949,691 ("Kurosaka")

Kurosaka teaches a logic circuit verification device that verifies the equivalence of two different logic circuits. Col. 2, lines 29-39. As part of the verification process, the device converts circuit data into a data file having a technology-independent intermediate data format. Col. 6, lines 31-35. The data file stores detailed circuit information for the two circuits that he wishes to compare using a point-detection algorithm. Col. 7, lines 6-16. No sequence of input signal vectors is represented by data file 106.

U.S. Patent No. 6,141,630 ("McNamara")

McNamara teaches a test generator that constructs a set of test vectors from a circuit design coded in a circuit design language. Col. 3, lines 22-43. The test generator interprets the circuit design as a series of blocks connected by transition arcs to form a state diagram, and constructs a first set of test vectors to cause each block to be visited and each transition arc to be taken. A second set of test vectors is also constructed to ensure user-selected transition paths are taken. Col. 4, lines 28-37. The data structures described by McNamara represent the circuit design. McNamara notes that a complete set of test vectors is called a test frame (Col. 4, line 66), but McNamara fails to teach or suggest how the test frame is represented.

U.S. Patent No. 5,684,808 ("Valind")

Valind teaches an automatic test pattern generator 56 that operates on a detailed circuit description 54 to generate test patterns. Fig. 4. The test pattern generator uses logic cone tracing and partitioning of the circuit logic to generate scan vectors that will detect stuck-at-1 and stuck-at-0 faults. Col. 9, lines 15-50. The examiner particularly cites the detailed circuit description 54 as anticipating applicant's claimed test pattern profile. However, as with Kurosaka and McNamara, the detailed circuit description and derivative data structures are used to represent the circuit design, and not a test pattern.

Issues

A prima facie case of obviousness requires, among other things, that the prior art reference (or references when combined) must teach or suggest al the claim limitations. Has the examiner established prima facie obviousness?

Grouping Of Claims

Claims 1-20 stand together.

Arguments

Applicants respectfully submit that the examiner erred in rejecting the claims under 35 USC § 103 because the art fails to teach or suggest all the claimed limitations.

To make a rejection under 35 U.S.C. § 103, the examiner must establish prima facie obviousness. *In re Oetiker*, 24 USPQ 2d 1443, 1444 (Fed. Cir. 1992). Section 2142 of the MPEP states:

> To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the

art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

Independent claim 1 recites in part: "a pattern profile that represents a sequence of input signal vectors with an associated sequence of output signal vectors (hereafter a "test pattern"). The examiner cites Kurosaka's teaching of an intermediate format data file 106 as anticipating a pattern profile that represents a test pattern. However, Kurosaka does not here or elsewhere teach or suggest the quoted element. To the contrary, Kurosaka teaches "The data file 106 in the intermediate format ... is provided ... to store detailed circuit information". Col. 7, lines 6-9. Kurosaka uses this file to store circuit information for two circuits that he wishes to compare using a point-detection algorithm. Col. 7, lines 12-16. No sequence of input signal vectors is represented by data file 106.

McNamara teaches a test generator that constructs a set of test vectors from a circuit design coded in a circuit design language. Col. 3, lines 22-43. The test generator interprets the circuit design as a series of blocks connected by transition arcs to form a state diagram, and constructs a first set of test vectors to cause each block to be visited and each transition arc to be taken. A second set of test vectors is also constructed to ensure user-selected transition paths are taken. Col. 4, lines 28-37. As with Kurosaka, the data structures represent the circuit design, and not a test pattern. The examiner cites, and applicant finds, no teaching or suggestion of a test pattern profile in McNamara.

Valind teaches an automatic test pattern generator 56 that operates on a detailed circuit description 54 to generate test patterns. Fig. 4. The test pattern generator uses logic cone tracing and partitioning of the circuit logic to generate scan vectors that will detect stuck-at-1 and stuck-at-0 faults. Col. 9, lines 15-50. The examiner cites the detailed circuit description 54 as anticipating

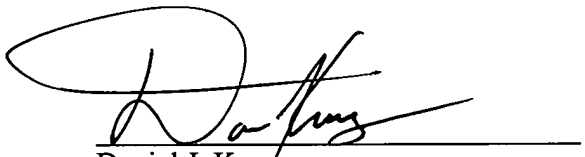
applicant's claimed test pattern profile. However, as with Kurosaka and McNamara, the detailed circuit description and derivative data structures are used to represent the circuit design, and not a test pattern.

Independent claims 11 and 17 also recite test pattern profiles as required elements. Applicant respectfully submits that independent claims 1, 11 and 17, along with their dependent claims, are allowable over the cited art for at least the reasons given above.

Conclusion

In light of the foregoing, applicants respectfully request that the examiner's rejections be reversed. If any fees are inadvertently omitted or if any additional fees are required or have been overpaid, please appropriately charge or credit those fees to LSI Logic Corporation Deposit Account Number 12-2252/5201-16301/DJK.

Respectfully submitted,



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CLAIMS

1. (Once amended) A system for device verification, wherein the system comprises

a profile generation module configured to provide a pattern profile that represents a sequence of input signal vectors with an associated sequence of output signal vectors (hereafter a "test pattern"), wherein the pattern profile includes a human-intelligible description of aspects of the test pattern, wherein the aspects are specified by a profile mode;

a coverage measurement module configured to process the pattern profile to produce analysis results indicative of coverage provided by the test pattern, wherein the profile generation module is further configured to process the analysis results to provide an improved pattern profile; and

a pattern generation module configured to receive the improved pattern profile and to convert the improved pattern profile into a test pattern for verifying device performance.

2. (Original) The system of claim 1, wherein the coverage measurement module is configured to determine coverage of the test pattern by ascertaining if node faults are detectable, wherein node faults are detectable if running the test pattern on a device would indicate a failure.

3. (Original) The system of claim 1, wherein the coverage measurement module ascertains if node faults are detectable for those nodes in a first category, and wherein the coverage measurement module ignores those nodes in a second category.

4. (Original) The system of claim 1, further comprising:

a test pattern profiling module configured to convert an existing test pattern into a pattern profile as specified by a profile mode.

5. (Original) The system of claim 1, further comprising:

a pattern checking module configured to process the pattern profile to produce analysis results indicative of whether the test pattern complies with a specified rule.

6. (Original) The system of claim 1, wherein the pattern generation module is coupled to run the test pattern on a device-under-test that implements at least a portion of a device design.

7. (Original) The system of claim 6, wherein the device design has a set of interesting input signals and a set of customary input signals, wherein the profile includes a human-intelligible representation of the set of interesting input signals, and wherein the profile does not include any representation of the set of customary input signals.

8. (Original) The system of claim 6, wherein the device design includes functional modules each having module input signals and module output signals.

9. (Original) The system of claim 8, wherein the profile includes a human-intelligible representation of a test pattern for one of the functional modules.

10. (Original) The system of claim 1, wherein the profile generation module is configurable to generate sequential permutations of values to specify pattern profiles.

11. (Once amended) A system for verifying device designs that include functional modules, wherein the system comprises:

a profile generation means for providing a pattern profile that represents a sequence of input signal vectors with an associated sequence of output signal vectors (hereafter

a "test pattern"), wherein the pattern profile includes an intelligible description of aspects of the test pattern, wherein the aspects are specified by a profile mode;

a coverage measurement means for analyzing the pattern profile to produce analysis results indicative of coverage provided by the test pattern, wherein the profile generation means is further configured to process the analysis results to provide an improved pattern profile; and

a pattern generation means for converting the improved pattern profile into a test pattern.

12. (Original) The system of claim 11, wherein the coverage measurement means is configured to determine coverage of the test pattern by ascertaining if node faults are detectable.

13. (Original) The system of claim 11, further comprising:

a test pattern profiling means for converting an existing test pattern into a pattern profile.

14. (Original) The system of claim 11, wherein the pattern generation means is coupled to run the test pattern on a device simulation means that implements at least a portion of a device design.

15. (Original) The system of claim 14, wherein the device design has a first set of input signals and a second distinct set of input signals, wherein the profile includes an intelligible representation of the first set of input signals, and wherein the profile does not include any representation of the second set of input signals.

16. (Original) The system of claim 14, wherein the device design includes functional modules each having module input signals and module output signals, and wherein the profile includes an intelligible representation of a test pattern for one of the functional modules.

17. (Once amended) A method for verifying a device design using a sequence of input signal vectors with an associated sequence of output signal vectors (hereafter a "test pattern"), wherein the method comprises:

analyzing a test pattern profile to determine coverage of a test pattern;

generating a second profile for an improved test pattern that provides better coverage;

converting the second profile into the improved test pattern; and

running the improved test pattern on a simulated device.

18. (Original) The method of claim 17, wherein the test pattern profile includes an intelligible representation of aspects of the test pattern, and wherein the aspects are specified by a profile mode.

19. (Original) The method of claim 18, wherein one aspect specified by the profile mode is a subset of input signals that represent instructions.

20. (Original) The method of claim 18, wherein one aspect specified by the profile mode is a set of input signals for a functional sub-module of the device design.